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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/753,103
Filing Date: January 06, 2004
Appellant(s): CHEN ET AL.

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For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/15/2007 appealing from the Office action mailed 5/15/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct. However, the amendment in which claims 3, 9, 10, 11, 17 and 21 were amended was filed on February 26, 2007, not on May 23, 2007 as erroneously stated in "Status of Claims" in the instant Appeal Brief.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct, although on page 1, "Summary of Claimed Subject Matter", line 8 of the first paragraph, "having a control gate (36)" should be replaced by "having a control gate (38)".

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,911,690	HSU ET AL.	6-2005
6,411,548	SAKUI ET AL.	6-2002
6,118,161	CHAPMAN ET AL.	09-2000

MATAS et al, "Memory 1997", ISBN: 1-877750-59-X; Section 10, "Flash Memory Technology", pages 10-1 through 10-6 (Integrated Circuit Engineering Corp.).

Appellant's Admitted Prior Art as contained in the Specification of Appellant's Application 10/753,103, "Background of the Invention" ([0003]-[0009], pp. 1-3) and Prior Art Figure 1.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-13, 15-22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al (6,911,690 B2) in view of either Prior Art as Admitted by Applicant in combination with Chapman (6,118,161) or Sakui et al (6,411,548) in combination with Chapman (6,118,161).

(10) Response to Argument

With regard to the independent claims 1, 15, 19 and 24:

Appellant's argument on pages 4-5 in support of the appeal of the rejection of claim 1 that "Examiner continues to misconstrue and mischaracterize what is actually found in the references, and he continues to try to combine selected elements from the different references (and now from Applicant's own disclosure) when there is no basis for doing so", and specifically that in Hsu et al there "are no bit lines, bit line diffusions or bit line contacts", appears to have missed the essence of the Response to Arguments ad 3), page 25 of the previous office action, where examiner provided evidence through Matas et al defining inter alia Flash Memory technology (Ch. 10), in particular the NAND Flash Memory Cell, that said bit lines, bit line diffusion and bit line contact are inherent in a NAND Flash Memory cell array (10-5 especially in Matas et al) while Hsu et al itself is quoted for the bit line diffusion (element 124) and Matas et al through page 10-5 specifically point out that the bit line is above the row and is seen to contact the bit line diffusion. There appears no reason at all to wonder, as Appellant does, why element 124 is a "bit line diffusion", this being a matter of words only. See Hsu et al, col. 8, l. 55 for evidence that the "drain" is part of a "bit line". That Hsu et al do not teach overlap is acknowledged in the rejection and hence requires no further commentary. The feature of a bit line diffusion is merely a drain region in the semiconductor connected to a bit line or bit line contact. This feature, i.e., a diffusion region connected to a bit line contact is, furthermore, in evidence as admitted prior art in Appellant's Specification, Prior Art Figure 1, as explained in the rejection contained in the Final Office Action. As to Appellant's question "where they (bit line and bit line contact) would they be (in Hsu et al)?', Appellant's Prior Art Figure 1 as well as the definition, of a NAND cell as provided

by Matas et al leave no doubt as where they would be, i.e., exactly where Appellant's inventive Figures 2 and 7 indicate they are, without any distinction at all (see Figures 2 and 7 in the Specification, and juxtapose with Prior Art Figure 1).

Counter to Appellant's argument on page 5 that "nowhere in the prior art is there any suggestion of bit line and source diffusions at opposite ends of a row of alternating stacked gates and select gates with no other diffusions in the active area between the bit line diffusion and the source region", between bit line diffusion 124 and source region 126 there are no other diffusion regions ("diffusions" in applicant words) in Hsu et al, while said alternating stacked gates and select gates are immediately evident in Hsu et al (see the cited 118/120 for stacked gates and 110 for select gates). Applicant asks: "Even if such elements (sic) were inherent in the device by Hsu et al, where would they be?" Interpreting "such elements" in the widest possible manner, this is where they are in the NAND Flash Memory Device by Hsu et al: bitline diffusion: 124, bitline contact inherently contacting said bitline diffusion by making contact to the upper main surface of said bitline diffusion (see Matas et al, page 10-5, Figure 10-8): downward bent portion of bitline (Aluminum)), and bitline: "Bitline (Aluminum) in Matas et al, straight portion overlying the plurality of alternating stacked gates 118/120 and select gates 110; and in the alternative rejection relying on Appellant's own admitted prior art, bitline diffusion 22, contacted by bitline contact 32 with bitline contiguous therewith and above the substrate (see Figure 1). No motivation is necessary because the only parts missing in Hsu et al in this regard are inherent in a NAND Flash Memory cell array as witnessed by Matas et al. As to applicant's question "how would the device work", NAND Flash Memory cell

arrays would NOT work in the absence of providing a bit line contact contacting the drain diffusion region alias bitline diffusion) to a bit line array. In a memory array bit lines provide the drain voltage to the drain diffusion regions connecting to said bit lines. Applicant appears to treat the rejection as if the elements shown by Hsu et al and those that are inherent in it according to Matas et al require some statement on motivation and combinability, in apparent misinterpretation of the role of Matas et al to show inherency of the bit line contact and bit line given the drain (= bit line diffusion) region in the NAND Flash Memory cell array by Hsu et al.

On Appellant's comment on Sakui et al (page 5, fourth paragraph) on the absence of even a remote suggestion of select gate - source diffusion overlap : Counter to Appellant's allegation (loc.cit.), Sakui et al does teach, gate-source-diffusion overlap for "a" transistor 27 (Figure 49 and col. 10, 63-64), while transistors 27 are either control transistors or select transistors (the latter indicated by "SSL" (see Fig. 31)). Therefore, counter to Appellant's allegation of inadequate teaching by Sakui et al, Sakui et al does teach the select gate to overlap source region 28d (Fig. 31). *Motivation* to include the teaching by Sakui et al in the invention by Hsu et al derives from the teaching by Chapman et al (col. 4, l. 21-28), which is known by those of ordinary skill in the art to apply to any field effect transistor as being beneficial by bringing down the resistance and hence cost (and undesirable heat) as well as performance (i.e., speed). Here, as everywhere else in applicant's discussion, it appears that a person of ordinary skill in the art merely would know how to spell words, and that when words selected by applicant are not spelled out then the limitation is not met. This is a gross underestimate

what is meant by "one of ordinary skill in the art", as also recently pointed out by the Supreme Court decision No. 04-1350 KSR International Co. v. Teleflex Inc et al; from which decision it is clear even more so than before that when a person of ordinary skill in the art could have combined Hsu et al with at least partial overlap of gate and select gate as disclosed by Sakui et al (see reference to col. 27, l. 43-49 in the previous office action) and would have seen the benefits of doing so (i.e., achieving low resistance and good performance as known in the art of insulated gate field effect transistors and witnessed for instance by Chapman et al (col. 4, l. 24-26). Anyone of ordinary skill in the art would consider the domain of advantage of low resistance to apply also to select gates: the operation of any gate takes less energy and time when operation is carried out under lower resistance, thus saving operation cost and enhancing performance through increasing speed. The alternative rejection based on appellant's admission of prior art, clearly shows said overlap as well (Fig. 1, select gate 31 overlapping source diffusion 23).

Appellant's position that the advantage of the select gate - source region overlap as taught by Chapman et al applies to MOSFETs but not a NAND flash memory cell is in error exactly because said teaching by Chapman et al is for any MOSFET, including those in the NAND flash memory device by Hsu et al: said select gate by Hsu et al IS a MOSFET, while the effect of gate-source overlap is even independent of the nature of the insulator and only rests on the short distance of gate surface to a region of increased mobility as provided by any diffusion region.

In conclusion, none of Appellant's arguments on pages 4-5 and repeated once more on page 6 in Appeal of the rejection of claim 1 are persuasive.

Appellant's arguments in support of his appeal of the rejections of other independent claims 15 and 19 do not distinguish over those set forth in support of the appeal of the rejection of claim 1, except that with regard to claim 15, "directly above" as interpreted by examiner is met if and only if a vertical line can be drawn that intersects both select gate and source diffusion, which is clearly the case in both Applicant's Admitted Prior Art (Figure 1) and Sakui et al (Figures 31 and 49). Examiner otherwise refers to his answer to the appeal of the rejection of independent claim 1 discussed above in this regard; while the plural rows as recited through claim 19 are in evidence in Hsu et al (Figure 1A) and discussion.

With regard to Appellant's argument (page 11) in support of his appeal of the rejection of claim 24, i.e., in traverse of examiner's position that alignment is in evidence (Hsu et al, Figure 1B), Appellant is referred to the discussion of Figure 1B (cols. 4-5), in particular that the setting of the select gates 110 "perpendicular to the active region 104" (col. 5, l. 12+) and the setting of the claimed stacked gates 118/120 "on the side and orthogonal to the active region 104" (col. 5, l. 26+) leaves no other conclusion than alignment. Furthermore, the limitation "self-aligned" rather than merely "aligned" only further introduces a limitation on the method of making said memory cell array and fails to further limit the invention claimed here as a final structure only. The distinction between "aligned" and "self-aligned" thus constitutes a product-by-process limitation

and is non-limiting. A product by process limitation is directed to the product per se, no matter how they are actually made. See MPEP 2113.

Furthermore, Appellant's argument that examiner's position that the voltage coupling from control and select gates to the floating gates is "unsupported and specious" (pages 11-12) appears oblivious of the operation of memory arrays relying on floating gates: select gates "select" control gates to be operative, while control gates control the flow of charge carriers (electrons) in and out of the floating gates. None of this is possible without voltage coupling between select and control gates on the one hand, and floating gates on the other hand.

In summary with regard to the independent claims, and referring to an overview in the form of a Table ("Table 1") provided as Appendix to this Examiner Answer, wherein "Y" designates teaching of the feature as claimed, and "N" means the absence of a specifically spelled-out teaching of said feature, Appellant's Appeal of the rejections of the independent claims 1, 15, 19 and 24 is found not to persuade.

With regard to the dependent claims:

Appellant's arguments on claim 2 (page 6), Appellant is referred to the discussion of Figure 1B (cols. 4-5), in particular that the setting of the select gates 110 "perpendicular to the active region 104" (col. 5, l. 12+) and the setting of the claimed stacked gates 118/120 "on the side and orthogonal to the active region 104" (col. 5, l. 26+) leaves no other conclusion than alignment. Furthermore, the limitation "self-aligned" rather than merely "aligned" only further introduces a limitation on the method of making said memory cell array and fails to further limit the invention claimed here as

a final structure only. The distinction between "aligned" and "self-aligned" thus constitutes a product-by-process limitation and is non-limiting. A product by process limitation is directed to the product per se, no matter how they are actually made. See MPEP 2113.

Appellant does not explain why cost considerations do not provide adequate motivation in the rejection of claim 3. Therefore, this argument on cost (page 6) is not persuasive. Furthermore, the very essence of a tunnel oxide is its thinness, so much so as to enable the wave function of the charge carrier to extend sufficiently across it to enable quantum-mechanical tunneling. Much effort has been made to make tunnel oxides of reliable thickness, or rather: thinness. No such requirement for the enablement of tunneling across any of the other dielectric layers makes any sense at all because only the movement in a controlled manner back and forth between channel (active layer) and floating gates benefits from a thickness small enough to enable tunneling. Therefore, Applicant's argument (page 6) that there is no basis for the examiner's argument that quantum mechanics mandates the claimed ordering in thickness is in error.

The limitation "surround" is not the essence of claim 4, being implied already by "plurality of stacked gates and select gates arranged alternately in a row" with "the stacked gate having a control gate positioned above a floating gate". Furthermore, "inter-gate capacitance" is in evidence in view of the relative position and isolation of said gates and by the very existence of inter-gate capacitance implies a coupling of the voltages and hence applicant's argument in appeal of claim 4 (pages 6-7) of this

rejection therefore fails to persuade. Appellant's argument appears, once again, oblivious of the distinction between using certain words and meeting the claim limitation.

Applicant's description of claims 5, 6 and 7 (page 7) and argument in appeal (page 7) on voltage coupling is the same as the argument discussed in the previous paragraph on claim 4 and the response must be the same, which is herewith included by reference. Furthermore, Appellant's argument on examiner's "unsupported argument that programming paths are allowed to exist because off-gate channel regions are conductive" (claim 6) and analogous argument on claim 7, completely ignores the very essence of how the NAND Flash Memory Cell Array enables programming (and erasure), namely: though the movement from the channel to the floating gates, respectively removal of electrons from the floating gates back into the channel. On Appellant's argument on voltage coupling (same paragraph) see preceding paragraph, herewith included by reference in response.

The alleged erring of examiner with regard to the rejection of claim 8 is not explained except through a reference to the determination of functional language or intended use; however, why biasing would not be a matter of use is not explained at all. Therefore, Appellant's argument of appeal of the rejections of claim 7-12 on this point is not persuasive (pages 7-9). Furthermore, Appellant in his argument in the final paragraph of page 7 fails to explain why the biasing of a specific element in a specific manner relative to other specific elements in a specific operational mode is "indeed" a structural limitation. The case law cited makes it clear that once the prior art is shown capable of performing the intended use then it meets the claim. Because of the tunnel

oxide and the available terminals to impart voltages on select and control gates, and because the floating gate have a floating potential, there is no doubt as to such capability; the more so since this capability is the very essence of the cell array's purpose.

The only point of specific traverse examiner can find in applicant's description of claims 16-19 is, at best, the allegation that the references "fail to disclose or even remotely suggest a memory cell array having these features", apparently in reference to the entire enumeration of claim limitations, for which examiner refers to the foregoing discussion, and perhaps to "memory cell array", for which it suffices to refer to the fact that Hsu et al teaches a NAND Flash Memory cell array (title, abstract and column 4, line 55- column 6, line 24, as mentioned in the previous action on the merits (page 17).

For the above reasons Appellant's arguments in support of the appeal of the rejections of the dependent claims are also deemed not to persuade.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Primary Examiner:

/Johannes Mondt (Art Unit: 3663)

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Meredith Petravick /MP/ Rick Palabrica /RP/

a/s: Appendix: Table 1.